HAWAII MR1: A New Underwater Mapping Tool

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Abstract

The HIG Acoustic Wide Angle Imaging Instrument, Mapping Researcher 1 (HAWAII MR1) is an ocean floor mapping sonar designed and built at the Hawaii Institute of Geophysics, of the University of Hawaii. Towed behind a ship at a depth of 100 meters, it is capable of measuring both acoustic back scatter reflectivity and bathymetry over a swath up to 25 km wide, in all ocean depths. This system is unique in that it incorporates a network of digital signal processors, in the tow vehicle and in the shipboard data acquisition electronics, which control tow vehicle operation and process the acquired data.

The tow vehicle carries two arrays of transducer elements; to reduce crosstalk, the port array operates at 11 kHz, while starboard uses 12 kHz. Each array consists of two rows of elements, spaced one-half wavelength apart. Both rows are driven by 10 kW amplifiers, transmitting sound pulses in the water 1 - 10 msec long. The transducer arrays are then used to receive reflected sound; the arrays' output passes through programmable gain amplifiers and then is digitized by dual channel 18 bit A/D converters.

The direction from which reflected sound arrives at the array is determined by measuring the phase difference between the two rows. The subsurface processors perform quadrature detection, followed by filtering matched to the transmitted pulse length; these data are then converted to block floating-point for telemetry to the surface.

At the surface, data are logged in this raw form, as well as processed for display. Bathymetry is calculated from the complex cross-product of the two rows' signals; after additional filtering, phase angles and travel time are converted to cross-track bathymetry. Complex magnitudes are corrected for spreading loss, attenuation, and beam pattern to produce a back scatter image. These images are displayed on a color monitor and on color and gray scale printers.

Digital signal processors reduce component count considerably, compared to previous systems; two printed circuit boards, each holding a DSP and 11 other integrated circuits, replace 35 printed circuit boards used in the first generation sonar of this type, SeaMARC II. All data acquisition and signal processing code is loaded from the surface; as the design also incorporates programmable gate arrays, the hardware configuration can also be modified remotely. Digital signal processing technology brings high performance, exceptional versatility, and enhanced reliability to this application.

Introduction

In 1981, researchers and engineers at the University of Hawaii Institute of Geophysics and at International Submarine Technology, Ltd., developed a unique seafloor mapping tool, called SeaMARC II. (Blackinton et al. 1983; Blackinton 1986) This was the first deep water sidescan sonar to measure the direction from which echoes arrived. This capability made it possible to determine the location of the bottom as well as its back scatter reflectivity, across a swath of seafloor as much as 10 km wide.

Prior to this time, ocean mapping sonar systems fell into two categories: sidescan sonars and multibeam sonars. Side scanning sonars radiate a fan-shaped beam of sound below and to the sides, and measure echoed signal strength, producing images of bottom back scatter reflectivity. Multibeam sonars use many transducers together with beam forming techniques to measure ranges for a number of different angles, to determine bathymetry over a swath across the ship's track.

SeaMARC II System Design

The SeaMARC II design was based on a conventional sidescan system, SeaMARC I, with additional electronics and by incorporating two horizontal rows of transducer elements on each side. A fan shaped beam of sound was

transmitted by the transducer arrays in the same way as previous sidescan systems, but by receiving the signals from the two rows independently, their phase difference could be measured, and the angle from which the sound arrived could be computed (Figure 1). This time series of angles, together with corrections for the velocity of sound in the survey water column, determine the location of the strip of sea bottom ensonified by that ping. At the same time, the time series of echo amplitudes can be converted to the conventional image of back scatter reflectivity.

The signal processing performed in the SeaMARC II system involved many steps; most were implemented using analog electronics. Signals from each row of transducer elements passed through preamplifiers, followed by two stages of time-varying-gain (TVG) amplifiers and one stage of operator controlled gain, to compensate for spreading loss and acoustic attenuation. Each signal was then multiplied by sine and cosine reference signals, at the carrier frequency; the products were low pass filtered and digitized at a 4 kHz rate and 12 bit resolution for telemetry to the surface. The signals from both rows were also summed to produce a single magnitude signal, compatible with the earlier SeaMARC I system; these electronics transmitted the signals to the surface using analog single sideband channels. Other sensors and circuitry measured tow vehicle attitude and depth, and transmitted these data to the surface.

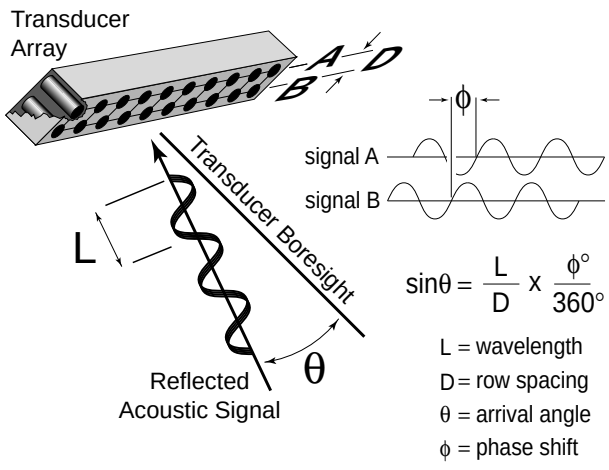

Figure 1. Diagram of the phase measuring technique used by both SeaMARC II and HAWAII MR1 for determining the arrival angle for sound reflected from the seafloor.

After arriving at the surface, the in-phase and quadrature components from each row were converted to angle and magnitude via a look-up table programmed into read-only memory. Samples with magnitudes exceeding threshold criteria for the two rows had their angles subtracted to calculate the phase difference. These phase differences were passed to a MicroPDP 11, where samples were binned and modal times picked for each phase angle difference. After magnitude signals were demodulated, they were applied to a bottom detect circuit that attempted to determine the first arrival of sound from the bottom; at that instant, analog/digital conversion of the magnitude signals would start. The sampling rate for these conversions was varied to produce samples evenly spaced in cross-track distance, based on the depth of the first arrival and the assumption that the entire swath was of the same depth. Prior to digitization, the magnitude signals passed through another gain stage whose gain was varied based on the bottom detection geometry, to compensate for transducer beam patterns and other cross-track variations. Slightly less than two thousand magnitude pixels were measured during a ping, each with 8 bit resolution, and logged on 9-track tape together with modal times picked for phase angles, under the control of another MicroPDP 11 computer. Realtime hardcopy output consisted of a gray scale graphic recorder for back scatter magnitude images and an ink jet color printer to display bathymetry.

The SeaMARC II system has been used extensively for a wide variety of seafloor mapping research, largely in the Pacific Ocean, but also in the Antarctic, Atlantic, Caribbean, and Norwegian Sea. Survey objectives have ranged from examining plate tectonics to sedimentation processes to determining routes for communication cables (Shor, 1990). The system was not without flaws, however. Most of the signal processing was done with analog electronics, with its inherent problems of component drift and failure. Apart from the two MicroPDP 11 computers, all digital logic was fabricated with SSI and MSI devices. The result was a system of formidable complexity; combined subsurface and shipboard electronics have nearly 100 printed circuit boards, thousands of components, and tens of thousands of interconnections. The early separation of acoustic data into amplitude and angle, followed by independent processing of both, simplified the electronic design but was less than ideal from a signal processing standpoint. Finally, the

requirement that the bottom return be detected in real time to trigger data acquisition led to data lost irretrievably when the bottom return was incorrectly identified.

A New Beginning

While the overall design concept of SeaMARC II remains useful and practical, the design implementation became outdated with the advent of digital signal processors. As these inexpensive and powerful microprocessors emerged on the marketplace, a number were evaluated to determine the core processor for the new system. The Motorola DSP56001 was selected, for its computational power, 24 bit word size, and its on-chip peripheral resources.

Solicitation of further information about this microprocessor led to discovering Motorola Inc.'s University Support Program, and ultimately to the generous donation by Motorola of a DSP56001 development system. This was very helpful for gaining experience with programming the 56001 and exploring its capabilities. In 1990 the US Naval Oceanographic Office expressed interest in acquiring a system similar in capability to SeaMARC II, and in September of that year funded the development of this new design, and construction of a sister system for their own use, now known as SEAMAP. In February 1991, the SeaMARC II tow vehicle was lost at sea while surveying in the South Pacific; the subsequent insurance recovery funded construction of HAWAII MR1.

HAWAII MR1 System Design - Hardware

The mechanical design of HAWAII MR1 is identical to that of SeaMARC II; in fact, a spare tow vehicle body and spare set of transducer arrays for SeaMARC II are now in use as HAWAII MR1. The tow vehicle itself is slightly positively buoyant, and houses the transducer arrays and subsurface electronics, packaged in two pressure housings. The vehicle is connected to a 2000 lb. depressor weight by an umbilical containing a single coaxial pair of conductors; the depressor in turn is towed behind the survey ship with an steel armored coaxial towing cable. Power for the subsurface electronics and telemetry signals are transferred via this coaxial pair of conductors.

A diagram of the subsurface electronics may be found in Figure 2. Two power amplifiers, each capable of 10 kW output power, drive the two rows of transducer elements on that side independently. Energy for the transmitted pulse is stored in capacitor banks and replenished by capacitor chargers drawing current directly from the high voltage (250 VDC) tow vehicle power. The transmitters' output is connected to a transmit/receive (T/R) circuit, transferring power from the power amplifiers to the transducers for transmission, then coupling transducer output to the preamplifiers for reception. The T/R circuit also contains voltage dividers and current transformers, producing signals which are digitized by the transmit monitor board, measuring transmitter output voltage and current.

Acoustic signals detected by the transducer arrays are passed by the T/R board to the preamplifier. The dual channel preamplifier contains a fixed 40 dB gain stage, followed by a variable gain stage with settings of 0 dB, 20 dB, 40 dB, and 60 dB. These amplified signals are then digitized on the A/D - D/A board. A Crystal Semiconductor CS5329 stereo A/D converter samples both signals simultaneously at 64 times their output sample rate, then performs digital filtering and decimation, resulting in 18 bit conversions at a sample rate of four times the carrier frequency, for each of the two signals. The output of the A/D is tagged with row identification bits and transmitted serially to the DSP. Data transfer is synchronous to A/D conversion, to minimize the effects of digital noise in the conversion output; all clocks on this board are derived from a crystal oscillator, running at 1024X the carrier frequency. This board also contains a Crystal CS4328 stereo D/A converter, whose output is used to inject calibration signals into the receiver, for monitoring system performance.

The serial digital data stream connects to a Xilinx 3042 Programmable Gate Array (PGA) on the DSP board. The output from the transmit monitor is also in serial form, and the PGA is programmed to multiplex the two into the DSP56001's Synchronous Serial Interface, or SSI. Memory for the DSP consists of 128 K words of zero wait state RAM, with 124 K in the DSP data space, and 4 K in the DSP program space. This board also houses an Analog Devices AD1341, an A/D Data Acquisition System on a chip. Configured for eight differential channels, it contains a multiplexer, programmable gain amplifier, and 12 bit digitizer. The analog channels are connected to pitch and roll sensors, a magnetic flux-gate heading sensor, a depth (hydrostatic pressure) sensor, voltage on both rows' capacitor banks, and towfish high voltage input power, leaving one spare channel. Finally, a boot EPROM contains code to start up the DSP and initialize the telemetry interface. The

electronics so far described are identical between the two sides; the sole differences between them are the frequency of crystal oscillators located on the A/D - D/A boards, and tuning components to match each side's arrays to the transmitters' output. The telemetry system is shared by both sides, and physically mounted in the starboard pressure housing. This telemetry system, manufactured by Colmek Systems Engineering, contains a half-duplex modem, capable of supporting data rates of up to 500 Kbaud. Data travels to and from the modem over a bidirectional RS-485 serial bus; a separate RS-422 line controls modem and bus data direction.

A diagram of the shipboard data acquisition system is shown in Figure 3. It is made up principally by a Sun Microsystems SPARC 2 workstation, with an S-bus coprocessor board from Berkeley Camera Engineering. The coprocessor board houses a Motorola DSP56001 and associated memory, a Xilinx 3042 PGA, and S-bus DMA interface hardware. The sole part of the topside electronics not purchased commercially is a box housing line drivers and receivers to convert TTL level signals from the coprocessor to RS-422 levels required by the telemetry system.

The surface telemetry modem uses the same modules as the subsurface modem. In addition, both surface and subsurface telemetry electronics contain circuitry to couple the FSK data to and from the cable that also transmits power to the tow vehicle. That power is provided by an Electronic Measurements Inc. power supply; power dissipation is typically less than 100 W.

In addition to the 200 Mb disk internal to the SPARC, two additional 650 Mb disks and two 8500 Exabyte tape drives are housed in an expansion box, connected to the SPARC's SCSI bus. A Raytheon TDU-850 gray scale graphic recorder and Tektronix Colorquick ink jet printer serve for hardcopy output.

HAWAII MR1 System Design - Software

A key component of the software design is the Serial Communication Interface (SCI) peripheral that is part of the DSP56001. This interface can be programmed for asynchronous multidrop communications, with separate data and address bytes (Motorola 1990). A relatively high speed (422 Kbaud) communications bus can be implemented using this mode of the SCI port on multiple DSP56001's. The port can be programmed to interrupt on address bytes only or on all bytes received. This capability forms the backbone of the new sonar system. Two processors located in the tow vehicle share this communication bus with another located in the surface data acquisition system.

The network protocol used in HAWAII MR1 is

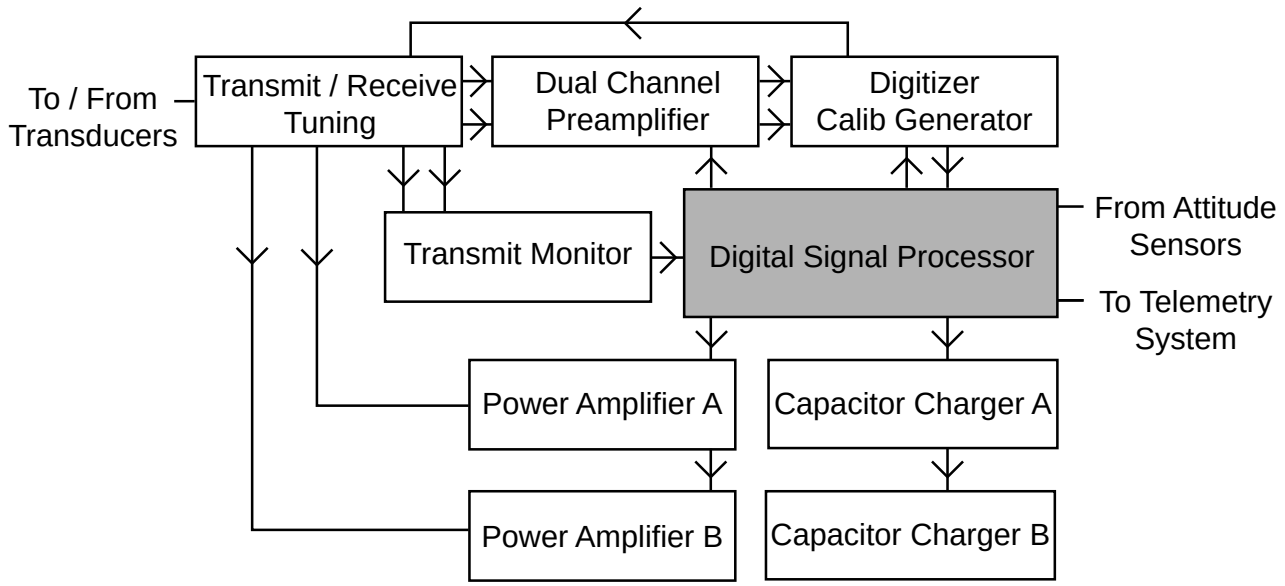

Figure 2. Schematic diagram of subsurface electronics for HAWAII MR1. Drawing illustrates one side only; electronics are identical on both port and starboard sides. Each block represents a single printed circuit board.

that the surface DSP is always master of the telemetry bus; subsurface processors are slaves. Commands are sent by the surface unit, which then releases control of the bus and waits for the subsurface processor addressed to acknowledge the command and respond. The surface DSP starts a timer when transmitting a command. If this timer expires before a response is heard, the topside assumes the command was not received, and resends it; after three attempts, the command is aborted, and an error is reported to the operator.

The present implementation uses four bits in the address word to indicate the processor address, allowing for up to 16 processors sharing the bus. The other four bits encode the type of command. Data associated with the command follows (for example, code to be loaded for future execution, or parameters to be used by the following ping). This sequence, called a packet, is terminated by a checksum and then an end-of-packet (EOP) flag, which also has a set address bit. In this way, packets are delimited at both ends by bytes with address bits on; all other bytes in a packet have the address bit cleared.

The slave processor, after receiving a valid (that is, checksum correct) packet, will acknowledge; the acknowledge message may include data, if the command was requesting it. The acknowledgment takes the form of a packet, with an initial address byte selecting the surface DSP, and ending with a checksum and EOP flag. If the packet checksum is not correct, the packet is discarded and a negative acknowledge, or NAK, is sent. The surface processor, upon receiving the NAK, will retransmit the last command packet; if it receives a data packet with an incorrect checksum, it will ask the subsurface DSP for that data again.

Upon powerup, the subsurface DSPs load boot code stored in the local EPROM that implements this telemetry protocol only. Code for controlling the tow vehicle electronics, acquiring and processing data, programming the gate array, etc. is loaded via the telemetry link. This makes software and firmware debugging and modification convenient; the high speed telemetry takes about a second to reload acquisition code and Xilinx programming.

A ping cycle begins when the subsurface is commanded to transmit. The subsurface processors control the transmit frequency and pulse length, using the receive digitizer clock as a timebase; this assures that transmit and receive timing and frequency are synchronous. Pulses may be transmitted having nominal lengths of 0.5, 1, 2, 5, and 10 msec; since the number of cycles transmitted is the same on both 11 and 12 kHz sides, 11 kHz pulses are slightly longer. While the transmitters are operating, their output voltage and current is sampled at a 80 kHz rate with 12 bit resolution, to measure transmitted power and monitor transmitter performance. After transmitting, the capacitor charging circuit is enabled, to replace energy in the capacitor storage banks. Data acquisition is begun, from both the acoustic digitizer and the attitude digitizer.

From a signal processing standpoint, HAWAII MR1 is very similar to SeaMARC II. Quadrature detection is used to extract phase and magnitude

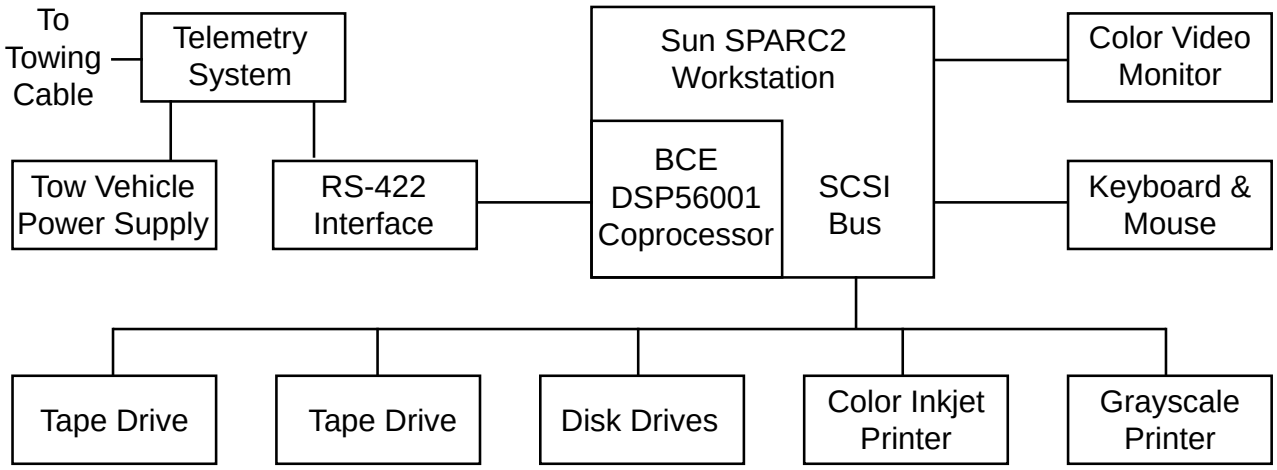

Figure 3. Schematic diagram of HAWAII MR1 surface electronics.

information from the received acoustic data. Almost all of this processing, however, is done digitally. The sole analog analog processing done is in the preamp, where gain can be changed in 20 dB steps. Immediately after transmitting, gain is at the minimum setting; the operator can select between a number of different schedules for increasing gain as a function of time since transmission.

The first step after digitization is to normalize the 18 bit output of the A/D converter to compensate for changes in analog gain. Since the conversion rate for each row is four times the transmit frequency, quadrature detection involves simply sorting and sign changing. The in-phase and quadrature components are then filtered digitally, using an FIR filter matched to the transmitted pulse length; since port and starboard transmit pulses are an equal number of cycles, the same filter coefficients are used for both sides. The filter output is decimated to a rate appropriate to the filter pass band, and the results collected into a packet of 256 samples. Once a packet is filled, it is converted from 24 bit values to block-floating point; each sample is represented by a 16 bit mantissa, and an 8 bit exponent for the entire packet.

After this conversion is complete, a checksum is added and the packet is marked to indicate its availability to the topside processor. This processor periodically requests completed packets from the subsurface processors, and when ready they are transferred via the telemetry system. Transmission errors are detected using the packet checksum; packets are retranmitted until received error-free. The large data space in the subsurface DSP memory can contain up to 8 seconds of acoustic data, so there is little danger of packets being overwritten by more recent data.

The topside processor buffers packets in its own memory for efficient DMA transfer to the SPARC memory. 500 msec before the time for the next transmission, the topside system halts data acquisition in the subsurface processors. During this time interval, attitude data packets are transferred, parameters for the next ping downloaded, and software executing on the SPARC transfers this raw data to disk. Once an hour new data are transferred from disk to tape, and data more than eight hours old are deleted from disk. Two tapes are recorded simultaneously, to provide redundant copies. Although the capacity of the tapes is much larger, normally six to eight hours of data are recorded on individual tapes. One very significant difference from previous sidescan systems is that all raw data are logged, from just after transmit until half a second before the next transmission; errors in determining the depth of nadir cause no loss of data, and are recoverable.

The data acquisition and display software runs within a windowing environment; the sonar operator may start and stop acquisition, change pulse width, transmit power, etc., by manipulating "buttons" and selecting from menus displayed on the SPARCstation color monitor. The Ethernet interface built into the workstation enables other machines on the network to access data as it is acquired.

Future Developments

One great advantage of the present DSP based design over the older one is the great flexibility it affords. Signal processing algorithms can be changed by simply editing and recompiling code. The use of programmable gate arrays for implementation of parts of the hardware adds significant flexibility there as well. We intend to take advantage of this flexibility in the near future to investigate other techniques in an attempt to further improve data quality.

Several standard procedures make it possible to increase the pulse length, and thus the total transmitted energy, of the transmitted sound without sacrificing spatial resolution in the reflected signal. These involve encoding the transmitted signal in various ways, by modulating its frequency or phase. While the pass band of our present transducer arrays place a limit on the range of frequency modulation possible, this approach may prove to be beneficial. Another possible improvement to be investigated is to steer the transmitted sound beam by manipulating the phase difference between the two rows' transmitters. When surveying shallow waters, more energy could be directed out to the side; in deep water, the transmit beam could be depressed.

Finally, the present system has been designed to permit easy expansion. The telemetry protocol will handle 13 additional DSP's on the network, and a straightforward revision would increase the total number to 256. The printed circuit boards carrying the DSPs in the subsurface electronics are designed with stacking connectors for the telemetry bus, power, DSP and PGA I/O pins; more processors can be simply plugged in to increase signal processing capability.

Acknowledgments

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