

MODULE Counters

TITLE 'Counters Frame Bit'

```
" define PALNAME ManchesterFrameBitCounter

" transition detector for HD-6408 emulator
" This decoder works with a clock rate of between 5 and 8 times the
" baud rate. Nominally the clock should be 6 times the baud rate.
" This rate was chosen for compatibility with the HD-6408 decoder rate,
" although it is possible to make a decoder with a slower clock.

rframe pin; " received left right\ frame
phaselx pin; " counter c1..c5 clock;
rmclk1x pin; " counter f1..f5 clock;

f5 pin istype 'reg'; " counter out bit
f4 pin istype 'reg'; " counter out bit
f3 pin istype 'reg'; " counter out bit
f2 pin istype 'reg'; " counter out bit
f1 pin istype 'reg'; " counter out bit
f0 pin istype 'reg'; " counter out bit

c48 pin istype 'reg'; " counter out bit
c16 pin istype 'reg'; " counter out bit
c1 pin istype 'reg'; " counter out bit

ff node istype 'reg'; " left right channel detect

f_cnt = [f5..f0];
```

EQUATIONS

```
ff.clk = (f_cnt == 32);
ff.aclr = rframe;

f0.clk = rmclk1x;
f1.clk = rmclk1x;
f2.clk = rmclk1x;
f3.clk = rmclk1x;
f4.clk = rmclk1x;
f5.clk = rmclk1x;
f0.aclr = rframe;
f1.aclr = rframe;
f2.aclr = rframe;
f3.aclr = rframe;
f4.aclr = rframe;
f5.aclr = rframe;

c1.clk = phaselx;
c16.clk = phaselx;
c48.clk = phaselx;

f_cnt := f_cnt+1;

ff := 1;

c1 := !ff;
c16 := (f_cnt == 16);
c48 := (f_cnt == 48);
```

END